

A Temperature Compensated Linear Diode Detector

Hans Eriksson
 Design Engineer
 Ericsson Radio Systems AB
 Kista, Sweden

Raymond W. Waugh
 Wireless Semiconductor Division
 Agilent Technologies
 Newark, California

Abstract: An AGC detector circuit is described which provides excellent temperature stability and linearity without the need for DC bias. Both simulated and measured data are presented.

Introduction

Schottky diodes find utilization as large signal detectors in AGC (automatic gain control) circuits in many applications. In his paper, Waugh^[1] describes a self-biased detector having good temperature stability at input power levels higher than 0 dBm, and describes the need for relatively high levels of DC bias to provide temperature compensation at lower input power levels. However, in order to separate the rectified output voltage (V_o) from the diode's forward bias voltage (V_f), these DC biased detector circuits require a differential amplifier and a reference diode which is carefully matched to the detector diode. Because of constraints on size and DC power, the self-biased detector is often a preferred approach.

The simple self-biased detector is shown in Figure 1.

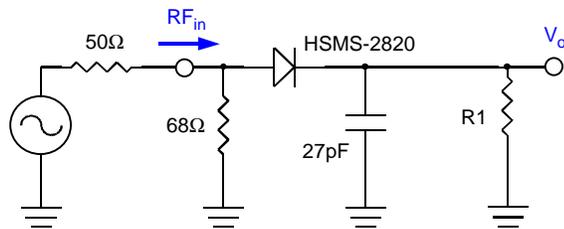


Figure 1: Self-biased detector

If the DC load resistor R1 is set to a relatively low value, such as 4.7KΩ, the Schottky diode will generate its own bias current at input power levels above 0 dBm. The 68Ω shunt resistor at the input to the diode provides for a wideband impedance match and a return path for the rectified (output) current.

When input power levels are low, the rectified current is insufficient to self-bias the diode, and the output voltage V_o varies with temperature, as can be seen in Figure 2. Not only is temperature stability poor at low levels of input power, but output linearity (tracking the ideal linear response) deteriorates as well.

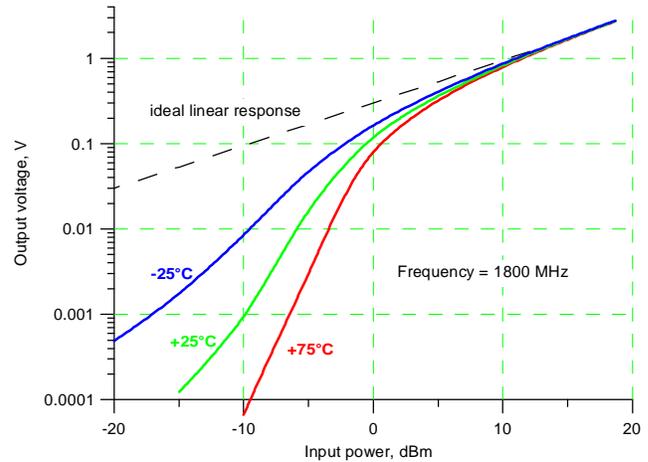


Figure 2: Measured performance of the self-biased detector

The reason for this variation can be explained as follows. The diode is a termination in the RF circuit (to the left of the 27pF capacitor in Figure 1). In the DC or output equivalent circuit, the diode can be modeled as a voltage source in series with the junction resistance R_j . Output voltage V_o can then be expressed as

$$V_o = V_{rectified} \frac{R1}{R1 + R_j} \quad (1)$$

where $V_{rectified}$ is the rectified voltage (open circuit V_o) and R1 is the DC load resistor shown in Figure 1. It can be seen that V_o will drop when $R_j \gg R1$.

In the small signal region, where rectified current is very small (-30 dBm or less), Schottky diode junction resistance is given by

$$R_j = \frac{nkT}{q(I_s + I_b)} \quad (2)$$

where n = diode ideality factor
 k = Boltzmann's constant
 T = temperature in degrees Kelvin
 q = the electronic charge
 I_s = diode saturation current
 I_b = external bias current

Saturation current for n-type Schottky detectors is very small -- for the HSMS-2820, it is typically 1.5×10^{-8} amperes. In this analysis, external bias current is zero. When these values are put into equation (2), the resulting value of junction resistance at room temperature is approximately $1.7\text{M}\Omega$. Since saturation current is highly temperature dependent^[2], R_j will be even higher at lower temperatures.

As input power is increased from -30 dBm, some circulating (rectified) current exists and the value of R_j goes down. A non-linear analysis can be used to calculate the value of R_j as a function of input power for the self-biased detector, as can be seen in Figure 3.

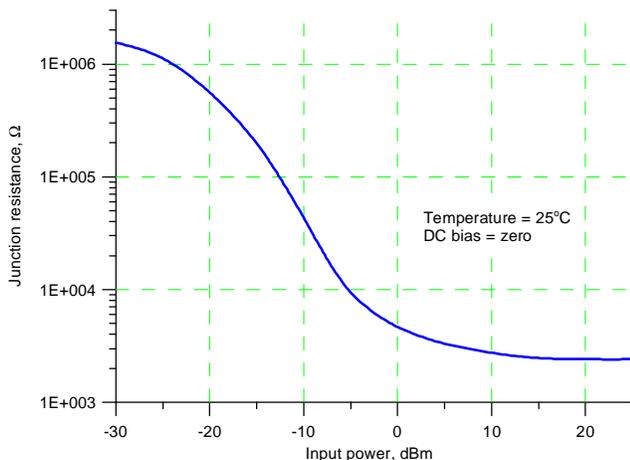


Figure 3: Junction resistance as a function of input power

In most detector applications, R_1 is in the range of $1\text{K}\Omega$ to $50\text{K}\Omega$. As can be seen when values of R_j from Figure 3 are plugged into equation (1), V_o will begin to deviate from the ideal linear response, and become temperature dependent, as input power levels drop below -5 dBm

Variable load circuit

An examination of equation (1) leads to the conclusion that a detector circuit with a variable load (R_1), one which tracks R_j , will result in improved temperature stability. Such a circuit is found in Figure 4. In this detector, a second diode, D_2 , is added in the DC portion of the circuit. The current produced by rectification in the detector diode, D_1 , also passes through D_2 . D_2 acts as a variable load resistor, following the relation given in equation (2). At low values of input power and/or ambient temperature, rectified current will be small, R_j in D_2 will be high and V_o will be increased compared to that in the simple detector of Figure 1.

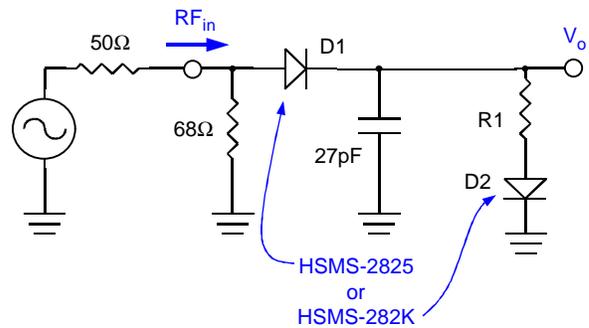


Figure 4: Detector with variable load resistance

When $R_1 = 4.7\text{K}\Omega$, the DC load presented to detector diode D_1 is shown in Figure 5.

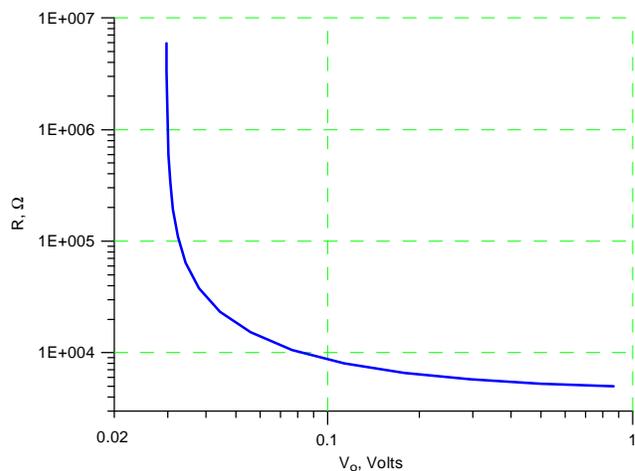


Figure 5: DC load resistance vs. detected voltage

If the DC circuit following the detector presents a sufficiently high resistance at the V_o output port ($R > 10^9\Omega$), temperature compensation will be achieved. An ADS^[3] analysis was performed on this circuit, with the results shown in Figure 6, for $R_1 = 4.7\text{K}\Omega$.

Comparing this transfer curve with that shown in Figure 2 illustrates the improvement in temperature stability, as well as detector linearity, at input power levels below 0 dBm. This circuit is useful at input power levels under -20 dBm, and offers a very large range of input power over which the output is constant with temperature.

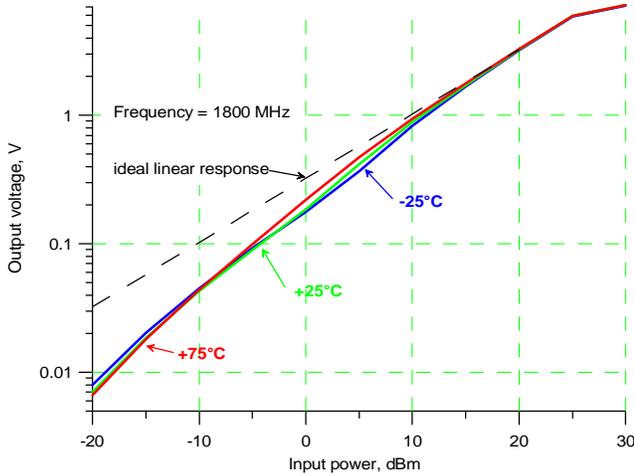


Figure 6: Transfer curve for the compensated detector

While the compensated detector of Figure 4 offers good temperature stability, certain applications might demand even better tracking to the ideal linear response (the dashed line in Figure 6). This might easily be accomplished by replacing the DC load in Figure 4 (R1 and D2) with a variable voltage divider, as shown in Figure 7.

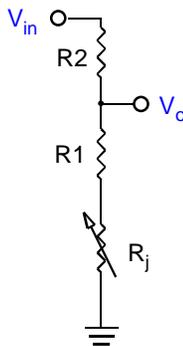


Figure 7: Variable voltage divider

R_j in this circuit is the current-controlled junction resistance of diode D2. At low values of detected signal (V_{in}), R_j will be very high and $V_o = V_{in}$. At high input power levels, which raise the value of rectified current and V_{in} , R_j will become small compared to R1 and R2. In the event that $R1 = R2$, $V_o = 0.5 V_{in}$. The result is that the output voltage shown in Figure 6 for $P_{in} = -20$ dBm are unaffected, while the higher output voltage ($P_{in} > 10$ dBm) are cut in half, improving linearity. The action of the variable voltage divider is shown in Figure 8 for the case in which $R1 = R2 = 4.7K\Omega$.

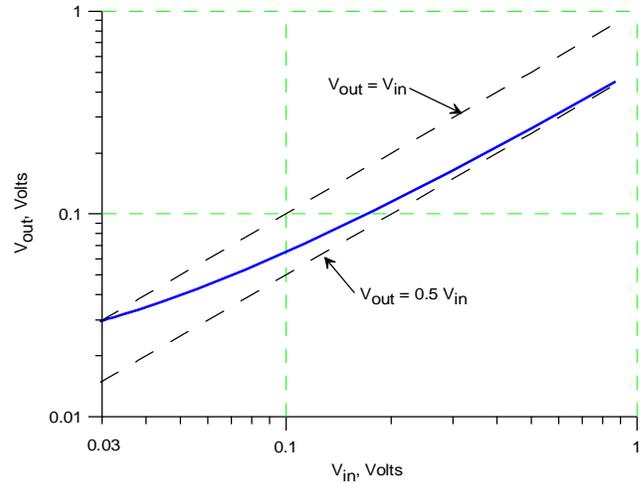


Figure 8: Performance of the variable voltage divider

The addition of this variable voltage divider to the circuit results in the linearized detector shown in Figure 9.

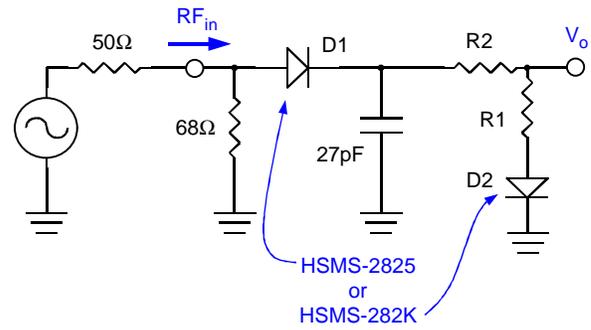


Figure 9: Linearized detector

It is this circuit which is the subject of this paper.

An ADS analysis of this detector results in the simulated transfer curve shown in Figure 10. Both R1 and R2 were set to $4.7K\Omega$. Comparing this performance with that given in Figure 6, one can immediately see the improvement in linearity, as well as some improvement in temperature stability. The simulation predicts almost perfect linearity and almost no variation with temperature for input power levels of -10 dBm or higher.

Design Tip

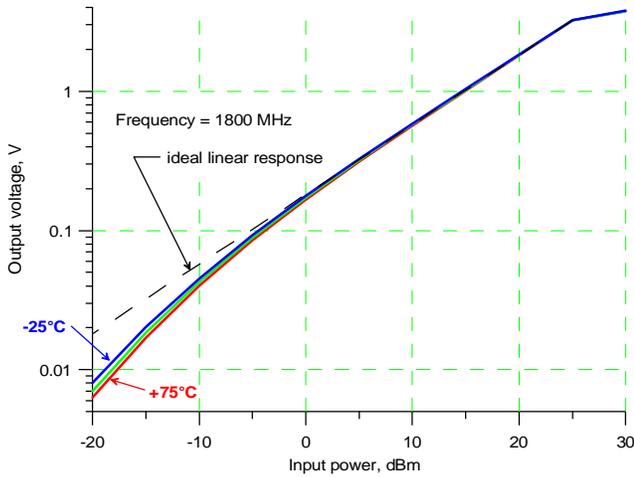


Figure 10: Simulated performance of the linearized detector

In order to verify the accuracy of the simulation, an experimental circuit was built and tested over temperature using the HSMS-2825 matched pair of diodes. The results are given in Figure 11.

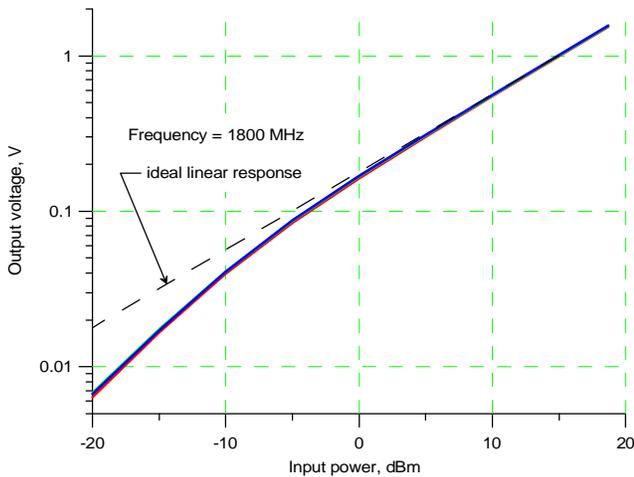


Figure 11: Measured performance of the linearized detector

The measured data shows slightly poorer linearity and slightly better temperature stability than predicted by the harmonic balance simulation. It is difficult to separate the three curves for -25°C, +25°C and +75°C in Figure 11. In all other respects, the data obtained in the lab correspond very closely to the ADS simulation.

The same circuit was simulated and tested at 900 MHz, with the results shown in Figure 12. As can be seen, linearity is excellent, as is the correspondence between simulation and experimental data.

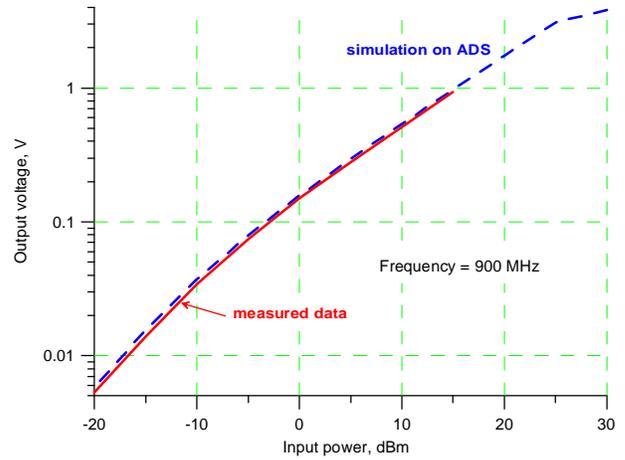


Figure 12: Measured vs. simulated performance at 900 MHz, 25°C

Figure 13 illustrates two possible physical layouts of the circuit. The first uses the HSMS-2826, a version of the HSMS-2825 with the polarity of one diode reversed, in the SOT-143 four-lead package. The second^[4] uses the SOT-363 six-lead HSMS-282K with its grounded center bar serving to provide RF isolation between the detector diode D1 and the compensating diode D2.

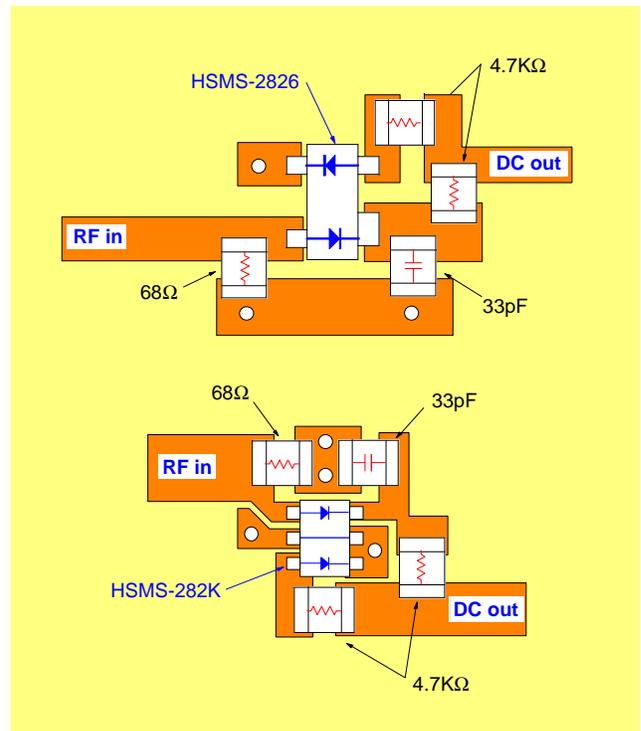


Figure 13: Circuit layouts

Conclusion

It has been shown that a simple detector, with two resistors and a diode in the load, can provide excellent temperature stability and linearity without the use of DC bias.

Correspondence between simulation and measured data has been shown to be excellent.

References

[1] Raymond W. Waugh, "Designing Large-Signal Detectors for Handsets and Base Stations," *Wireless Systems Design*, Vol. 2, No. 7, July 1997, pp 42 – 48.

[2] Raymond W. Waugh and Rolando R. Buted, "The Zero Bias Schottky Diode Detector at Temperature Extremes - Problems and Solutions," *Proceedings of the WIRELESS Symposium*, 1996, pp 175 - 183

[3] Agilent Technologies *Advanced Design System*

[4] Private communication with Alan Rixon, Agilent Technologies